REMARKS

In the Official Action mailed on **April 2, 2004**, the examiner reviewed claims 1-24. Claims 1-24 were rejected under 35 U.S.C. §112, first paragraph as failing to comply with the written description requirement. Claims 1-24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Marcuello et al. (*Value Prediction for Speculative Multithreaded Architectures*, hereinafter "Marcuello (1)") and further by Marcuello et al. (*Speculative Multithreaded Processors*, incorporated by reference in Section 2 of *Value Prediction for Speculative Multithreaded Architectures*, hereinafter "Marcuello (2)") in view of Shiell et al. (USPN 5,850,543, hereinafter "Shiell), further in view of Patterson et al. (*Computer Organization & Design: The Hardware/Software Interface*, hereinafter "Patterson").

Rejections under 35 U.S.C. §112, first paragraph

Claims 1-24 were rejected under 35 U.S.C. §112, first paragraph as failing to comply with the written description requirement.

Applicant has amended independent claims 1, 12, and 23 to remove the non-supported material cited by the Examiner.

Rejections under 35 U.S.C. §103(a)

Independent claims 1, 12, and 23 were rejected as being unpatentable over Marcuello (1) and further by Marcuello (2) in view of Shiell, further in view of Patterson. Applicant respectfully points out that Marcuello (1) and (2) teaches comparing the **final** results of the head thread and the speculative thread and either rolling back the speculative thread or committing the speculative thread, depending on the result of the comparison (see Marcuello (2), col. 8, lines 7-11, and col. 4, lines 53-57).

In contrast, the present invention is directed to **monitoring every write operation** from the head thread to determine if the speculative thread has read the value and, if so, immediately rolling back the speculative thread to reread the new value (see FIGs. 5, and 7-8, page 13, line 19 to page 14, line 11, and page 15, line 14 to page 16. line 18 of the instant application). It is advantageous to monitor every write operation from the head thread to determine if the speculative thread has read the value and, if so, immediately rolling back the speculative thread to reread the new value because an error can be detected earlier. Detecting an error earlier prevents the system from continuing execution of a speculative thread using incorrect data, thereby providing better utilization of the speculative thread.

There is nothing within Marcuello (1), Marcuello (2), Shiell, or Patterson, which suggests monitoring every write operation from the head thread to determine if the speculative thread has read the value and, if so, immediately rolling back the speculative thread to reread the new value.

Accordingly, Applicant has amended independent claims 1, 12, and 23 to include limitations from dependent claims 10-11 and 21-22 to clarify that the present invention monitors every write operation from the head thread to determine if the speculative thread has read the value and, if so, immediately rolls back the speculative thread to reread the new value. Dependent claims 10-11 and 21-22 have been canceled without prejudice.

Hence, Applicant respectfully submits that independent claims 1, 12, and 23 as presently amended are in condition for allowance. Applicant also submits that claims 2-9, which depend upon claim 1, claims 13-20, which depend upon claim 12, and claim 24, which depends upon claim 23, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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